R20

Code No: R20A0506

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Supplementary Examinations, June 2025

Computer Organization

(CSE, CSE-CS, CSE-AIML & B.Tech-AIML)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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			BCLL	CO(s)	Marks
		SECTION-I			
1	***A***	Demonstrate how data is transferred between the CPU and RAM using a bus structure.	**L3**	**CO-I**	**[7M]**
	B	Compare two's complement and one's complement in terms of representation and arithmetic operations.	**L4**	**CO-I**	**[7M]**
		OR			
2	***A***	Compare the roles of registers and cache in improving the performance of a computer.	**L2**	**CO-I**	**[7M]**
	B	Analyze the difference between fixed-point and floating-point representations.	**L4**	**CO-I**	**[7M]**
		SECTION-II			
3	***A***	Explain the significance of Register Transfer Language in describing computer operations.	**L2**	**CO-II**	**[7M]**
	B	Analyze how shift micro-operations are used in binary systems.	**L4**	**CO-II**	**[7M]**
		OR			
4	***A***	Illustrate the difference between arithmetic and logical micro-operations with examples.	**L2**	**CO-II**	**[7M]**
	B	Explain the instruction cycle of a CPU, detailing the fetch, decode and execute.	**L2**	**CO-II**	**[7M]**
		SECTION-III			
5	***A***	Describe the different addressing modes used in instruction sets with examples. Why are addressing modes important for efficient programming?	**L4**	**CO-III**	**[7M]**
	B	Describe the differences between direct addressing and indirect addressing in the context of address sequencing.	**L2**	**CO-III**	**[7M]**
		OR			
6	***A***	Illustrate the role of data transfer in executing an instruction within a CPU with an example.	**L3**	**CO-III**	**[7M]**
	B	Demonstrate how the control unit interacts with other components of the CPU during instruction execution.	**L2**	**CO-III**	**[7M]**
		SECTION-IV			
7	***A***	Describe memory hierarchy in a computer system. Why is caching important in the memory hierarchy?	**L2**	**CO-IV**	**[7M]**

	B	Define page fault. Explain briefly about any two page replacement algorithms with suitable examples.	**L3**	**CO-IV**	**[7M]**
		OR			
8	***A***	Compare associative memory with traditional memory in terms of access time, flexibility, and complexity.	**L4**	**CO-IV**	**[7M]**
	B	You have 3 page frames available and the following page reference string: 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2 a) Use the Optimal page replacement algorithm to determine how many page faults occur. b) Explain why this algorithm is considered "optimal" and provide a comparison with FIFO and LRU based on the number of page faults.	**L3**	**CO-IV**	**[7M]**
		SECTION-V			
9	***A***	Explain the role of peripheral devices in expanding the functionality of a computer system.	**L2**	**CO-V**	**[7M]**
	B	Compare the impact of different types of hazards (data, structural, control) on the throughput of a pipelined CPU.	**L4**	**CO-V**	**[7M]**
		OR			
10		Discuss about DMA technique in detail.	**L2**	**CO-V**	**[14M]**

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